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| Test ID | Test Priority | Test summary | Preconditions | Test Steps | Test Data | Expected Results | Actual Results | Test Status (Pass/Fail) |
| TC\_RST\_001 | High | It ensures the reset functions woks well | It doesn’t require precondition state | Applying rst\_n signal asynchronously to DUT | Active low reset signal | All output signals  is zero |  |  |
| TC\_REQ\_CPU1\_002 | High | Ensuring handling the request from Processor 1 | It requires the MCC in IDLE State. | Applying the request signal to MCC and observing the output | -posedge clk  -req\_1=1’b1 -rst\_n=1’b1 | Access granted for CPU1 through grant\_1=1’b1 |  |  |
| TC\_REQ\_CPU1\_003 | High | Ensuring handling the request from Processor 2 | It requires the MCC in IDLE State. | Applying the request signal to MCC and observing the output | posedge clk  req\_2=1’b1 rst\_n =1’b1 req\_1=1’b0 | Access granted for CPU2 through grant\_2=1’b1 |  |  |
| TC\_WR\_CPU1\_004 | High | Write operation for CPU1 | It requires the MCC in IDLE State | Applying the request signal to gain access with write signal and data driven to memory and address specified for completing write operation | Posedge clk req\_1=1’b1  Rw\_1=1’b1 addr\_1=any data\_in\_1=any rst\_n = 1’b1 | Grant\_1=1’b1 data\_out\_1=’h0 mem\_addr =addr\_1  Mem\_rw=RW\_1 mem\_data\_in =data\_in\_1 mem\_data\_out=1’b0 |  |  |
| TC\_WR\_CPU2\_005 | High | Write operation for CPU2 | It requires the MCC in IDLE State | Applying the request signal to gain access with write signal and data driven to memory and address specified for completing write operation | Posedge clk req\_2=1’b1  Rw\_2=1’b1 addr\_2=any data\_in\_2=any rst\_n = 1’b1 req\_1=1’b0 | Grant\_2=1’b1 data\_out\_2=’h0 mem\_addr =addr\_2  Mem\_rw=RW\_2 mem\_data\_in =data\_in\_2 mem\_data\_out=1’b0 |  |  |
| TC\_RD\_CPU1\_006 | High | Read operation for CPU1 | It requires the MCC  in IDLE State | Driving the request signal with appropriate address for read | Posedge clk  req\_1=1’b1 RW\_1=1’b0 addr\_1=specified data\_in\_1=’hx rst\_n=1’b1 | Grant\_1=1’b1 data\_out\_1=mem[addr] mem\_addr=addr\_1 mem\_rw=RW\_1 mem\_data\_in=’hx mem\_data\_out=mem[addr] |  |  |
| TC\_RD\_CPU1\_007 | High | Read operation for CPU2 | It requires the MCC  in IDLE State | Driving the request signal with appropriate address for read | Posedge clk  req\_2=1’b1 RW\_2=1’b0 addr\_2=specified data\_in\_2=’hx rst\_n=1’b1 | Grant\_2=1’b1 data\_out\_2=mem[addr] mem\_addr=addr\_2 mem\_rw=RW\_2 mem\_data\_in=’hx mem\_data\_out=mem[addr] |  |  |
| TC\_Cpu1Cpu2Acess\_008 | High | Concurrent Access for two processors handling priority | It requires the MCC in IDLE state or LOW\_POWER\_MODE | Driving the request from both processors | Posedge clk  req\_1=1’b1 req\_2=1’b1 rst\_n=1’b1 | Grant\_1=1’b1 Grant\_2=1’b0 |  |  |
| TC\_LOWPOWER\_008 | Medium | Ensuring Low power state when no access for a long time | It requires the state idle stayed for 10 clock cycles | No signals for 10 cycles | Posedge clk  rst\_n=1’b1 | none |  |  |